CLAIMS

1. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio; and

said first etch/dep ratio is selected to be higher than said second etch/dep ratio.

2. The method as claimed in claim 1 wherein said trench comprises a shallow trench isolation trench.

3. The method as claimed in claim 1 wherein said trench comprises an intermetal dielectric trench.

4. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein:

said trench has an aspect ratio between about 6:1 to about 10:1;

said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio; and

said first etch/dep ratio is selected to be higher than said second etch/dep ratio.

5. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio;

said first etch/dep ratio is selected to be higher than said second etch/dep ratio; and

said first gas flow is selected to have a rate of flow lower than a rate of flow of said second gas flow.

6. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio;

said first etch/dep ratio is selected to be higher than said second etch/dep ratio; and

said first RF bias is higher than said second RF bias.

7. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio;

said first etch/dep ratio is selected to be higher than said second etch/dep ratio;

said first gas flow is selected to have a rate of flow lower than a rate of flow of said second gas flow; and

said first RF bias is higher than said second RF bias.

8. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein:

said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio; and

said first layer of trench filling material partially fills trench such that said first layer of trench filling material has a substantially v-shaped upper surface profile;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio;

said first etch/dep ratio is selected to be higher than said second etch/dep ratio; and

said first gas flow is selected to have a rate of flow lower than a rate of flow of said second gas flow; and

said first RF bias is higher than said second RF bias.

9. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber, wherein said first gas flow comprises at least one first silicon containing gas, at least one first oxygen containing gas, and at least one first inert gas;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein:

said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio; and

said first layer of trench filling material comprises silicon dioxide;

flowing a second gas flow into said process chamber, wherein said second gas flow comprises at least one second silicon containing gas, at least one second oxygen containing gas, and at least one second inert gas;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio;

said first etch/dep ratio is selected to be higher than said second etch/dep ratio; and

said second layer of trench filling material comprises silicon dioxide.

10. The method as claimed in claim 9 wherein said first inert gas is selected from hydrogen, deuterium, argon, helium, and neon, and combinations thereof.

11. The method as claimed in claim 9 wherein said first inert gas comprises hydrogen.

12. The method as claimed in claim 9 wherein said second inert gas is selected from hydrogen, deuterium, argon, helium, and neon, and combinations thereof.

13. The method as claimed in claim 9 wherein said second inert gas comprises hydrogen.

14. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber, wherein said first gas flow comprises a first silane gas, a first oxygen gas, and a first hydrogen gas;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein:

said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio; and

said first layer of trench filling material comprises silicon dioxide;

flowing a second gas flow into said process chamber, wherein said second gas flow comprises a second silane gas, a second oxygen gas, and a second hydrogen gas;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio;

said first etch/dep ratio is selected to be higher than said second etch/dep ratio; and

said second layer of trench filling material comprises silicon dioxide.

15. The method as claimed in claim 14 wherein:

said first silane gas has a flow rate of between about 10 to about 35 sccm;

said first oxygen gas has a flow rate of between about 20 to about 65 sccm; and

said first hydrogen gas has a flow rate of between about 100 to about 1200 sccm.

16. The method as claimed in claim 15 wherein said first RF bias is above about 1000 W.

17. The method as claimed in claim 14 wherein

said second silane gas has a flow rate of between about 35 to about 70 sccm;

said second oxygen gas has a flow rate of between about 65 to about 100 sccm; and

said second hydrogen gas has a flow rate of between about 100 to about 1200 sccm.

18. The method as claimed in claim 17 wherein said second RF bias is below about 3000 W.

19. The method as claimed in claim 14 wherein:

said first silane gas has a flow rate of between about 10 to about 35 sccm;

said first oxygen gas has a flow rate of between about 20 to about 65 sccm;

said first hydrogen gas has a flow rate of between about 100 to about 1200 sccm;

said second silane gas has a flow rate of between about 35 to about 70 sccm;

said second oxygen gas has a flow rate of between about 65 to about 100 sccm; and

said second hydrogen gas has a flow rate of between about 100 to about 1200 sccm.

20. The method as claimed in claim 19 wherein said first RF bias is above about 1000 W, and wherein said second RF bias is below about 3000 W.

21. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein:

said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio;

said first layer of trench filling material partially fills trench such that said first layer of trench filling material has a substantially v-shaped upper surface profile;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio; and

said first etch/dep ratio is selected to be higher than said second etch/dep ratio.

22. A method of filling shallow trench isolation trenches in a semiconductor substrate located in a process chamber, comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor substrate, wherein said first gas flow and said first RF bias are selected such that said shallow isolation trenches are partially filled with a first layer of trench filling material at a first etch/dep ratio;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor substrate, wherein:

said second gas flow and said second RF bias are selected such that said shallow trench isolation trenches are filled with a second layer of trench filling material at a second etch/dep ratio; and

said first etch/dep ratio is selected to be higher than said second etch/dep ratio.

23. A method of filling shallow trench isolation trenches in a semiconductor substrate located in a process chamber, comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor substrate, wherein:

each of said shallow isolation trenches is defined by a pair of sidewalls and a trench bottom and has a nitride liner layer proximate to said sidewalls and said trench bottom; and

said first gas flow and said first RF bias are selected such that said shallow isolation trenches are partially filled with a first layer of trench filling material at a first etch/dep ratio;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor substrate, wherein:

said second gas flow and said second RF bias are selected such that said shallow trench isolation trenches are filled with a second layer of trench filling material at a second etch/dep ratio;

said first etch/dep ratio is selected to be higher than said second etch/dep ratio;

said nitride liner layer is not substantially eroded during the filling of said shallow isolation trenches with said first layer of trench filling material; and

said nitride liner layer is not substantially eroded during the filling of said shallow isolation trenches with said second layer of trench filling material.

24. A method of filling shallow trench isolation trenches in a semiconductor substrate located in a process chamber, comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor substrate, wherein:

said first gas flow and said first RF bias are selected such that said shallow isolation trenches are partially filled with a first layer of trench filling material at a first etch/dep ratio; and

said first layer of trench filling material partially fills said shallow trench isolation trenches such that said first layer of trench filling material has a substantially v-shaped upper surface profile;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor substrate, wherein:

said second gas flow and said second RF bias are selected such that said shallow trench isolation trenches are filled with a second layer of trench filling material at a second etch/dep ratio; and

said first etch/dep ratio is selected to be higher than said second etch/dep ratio.

25. A method for filling a trench in a semiconductor layer located in a process chamber comprising:

flowing a first gas flow into said process chamber;

forming a first plasma from said first gas flow;

applying a first RF bias to said semiconductor layer, wherein:

said trench has an aspect ratio between about 6:1 to about 10:1;

said first gas flow and said first RF bias are selected such that said trench is partially filled with a first layer of trench filling material at a first etch/dep ratio;

said first layer of trench filling material partially fills said trench such that said first layer of trench filling material has a substantially v-shaped upper surface profile;

flowing a second gas flow into said process chamber;

forming a second plasma from said second gas flow; and

applying a second RF bias to said semiconductor layer; wherein:

said second gas flow and said second RF bias are selected such that said trench is filled with a second layer of trench filling material at a second etch/dep ratio; and

said first etch/dep ratio is selected to be higher than said second etch/dep ratio.

26. A method of filling trenches in a semiconductor layer by HDP-CVD, comprising:

forming a first plasma from a first gas flow, wherein said first gas flow has a flow rate;

applying a first RF bias to said semiconductor layer;

exposing said semiconductor layer to said first plasma, wherein:

said step of exposing said semiconductor layer to said first plasma causes deposition of a first layer of trench filling material in said trenches; and

said first gas flow rate and said first RF bias are selected such that said deposition of said first layer of trench filling material occurs at a first etch/dep ratio;

forming a second plasma from a first gas flow, wherein said second gas flow has a flow rate;

applying a second RF bias to said semiconductor layer;

exposing said semiconductor layer to said second plasma, wherein:

said step of exposing said semiconductor layer to said plasma causes deposition of a second layer of trench filling material in said trenches;

said second gas flow rate and said second RF bias are selected such that said deposition of said second layer of trench filling material occurs at a second etch/dep ratio; and

said first etch/dep ratio is selected to be higher than said second etch/dep ratio.

27. The method as claimed in claim 26 wherein said first etch/dep ratio is selected to be above about 0.3.

28. The method as claimed in claim 26 wherein said second etch/dep ratio is selected to be below about 0.3.

29. A method of forming a silicon dioxide layer filling trenches in a semiconductor layer by HDP-CVD, comprising:

forming a first plasma from a first gas flow, wherein said first gas flow comprises a silicon containing gas, an oxygen containing gas, and an inert gas, and wherein said first gas flow has a flow rate;

applying a first RF bias to said semiconductor layer;

exposing said semiconductor layer to said first plasma, wherein:

said step of exposing said semiconductor layer to said first plasma causes deposition of a first layer of silicon dioxide in said trenches; and

said first gas flow rate and said first RF bias are selected such that said deposition of said first layer occurs at a first etch/dep ratio;

forming a second plasma from a first gas flow, wherein said second gas flow comprises a silicon containing gas, an oxygen containing gas, and an inert gas, and wherein said second gas flow has a flow rate;

applying a second RF bias to said semiconductor layer;

exposing said semiconductor layer to said second plasma, wherein:

said step of exposing said semiconductor layer to said plasma causes deposition of a second layer of silicon dioxide in said trenches;

said second gas flow rate and said second RF bias are selected such that said deposition of said second layer occurs at a second etch/dep ratio; and

said first etch/dep ratio is selected to be higher than said second etch/dep ratio.